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| 10/761,319 | 01/22/2004 | Howard E. Rhodes | M4065.0107/P107-F | 2671 |

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| EXAMINER | |
|---|---|
| CHEN, CHIA WEI A | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/761,319 | RHODES ET AL. | |
| | Examiner | Art Unit | |
| | CHIA-WEI A. CHEN | 2622 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *70-79 and 120-130* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *70-79 and 120-130* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 70-79 and 120-130 have been considered but are moot in view of the new ground(s) of rejection.

### *Double Patenting*

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 70-79 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 36-79 of U.S. Patent No. 6,310,366. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application claims are broader in every aspect than the patent claim and is therefore an obvious variant thereof.

4. Claims 120-130 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 20-35 of U.S. Patent No. 6,310,366 in view of Fossum (U.S. Patent No. 5,471,515).

Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 120 is generic and only further discloses an active pixel sensor structure that is well known in the art.

Claim 120, U.S. Patent No. 6,310,366 claim 20 discloses an imager comprising:

an array of pixel sensor cells formed in a retrograde well in a substrate, the retrograde well being doped with a vertically graded dopant concentration, wherein each of said pixel sensor cells is separated by an isolation region that electrically isolates said pixel cells from each other, and each said pixel sensor cell comprising comprises:

a photoconversion device;

but is silent regarding:

a reset transistor;

a source follower transistor;

a row select transistor; and

a floating diffusion region in electrical communication with said photoconversion device and said source follower transistor.

Fossum teaches a reset transistor (45); a source follower transistor (55); a row select transistor (60); and a floating diffusion region (40) in electrical communication with said photocoversion device and said source follower transistor (Fig. 1; col. 3, lines 7-21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the Active Pixel Sensor structure of Fossum with the imager of U.S. Patent 6,310,366 to form an imager that consumes less power and has less image lag than a typical CMOS imager.

***Claim Rejections - 35 USC § 103***

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 70, 120, and 122-124 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark (US 5,859,450) in view of Mundt (US 4,578,128).

Claim 70, Clark teaches, in Fig. 1, an imager comprising:

- an array of pixel sensor cells wherein each pixel sensor cell has a photosensitive region and a photosensor formed at the photosensitive region, and
- a circuit (Fig. 6) formed in the substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing the image (output to image capture system; col. 5, lines 20-23); and
- a processor (609) for receiving and processing data representing the image (col. 5, lines 13-16);

but does not teach wherein the array is formed in a retrograde well on a substrate, the retrograde well being doped with a vertically graded dopant profile.

Mundt teaches a retrograde well in a substrate, the retrograde well being doped with a vertically graded dopant concentration (52P, 52N of Fig. 8, col. 5, lines 27-33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the retrograde doped substrate with the imager of Clark since retrograde dopant distribution in semiconductor substrates have the potential of increased device packing density and decreased susceptibility to latchup. (See col. 1, lines 15-20 of Mundt.)

Claim 120, Clark teaches, in Figure 6, a CMOS imager comprising:

- an array of pixel sensor cells each of said pixel sensor cells being separated by an isolation region that electrically isolates said pixel cells from each other (col. 2, lines 54-58; col. 4, lines 13-20), and each said pixel sensor cell comprising:
- a photoconversion device (602);
- a reset transistor (614);
- a source follower transistor (616);
- a row select transistor (622); and
- a floating diffusion region (618) in electrical communication with said photoconversion device and said source follower transistor (col. 5, lines 8-30).

Mundt teaches a retrograde well in a substrate, the retrograde well being doped with a vertically graded dopant concentration (52P, 52N of Fig. 8, col. 5, lines 27-33).

Claim 123, Clark teaches wherein the photoconversion device is a photodiode (col. 2, lines 50-51).

Claims 122 and 124, Clark in view of Mundt discloses substantially the claimed invention as set forth in the discussion for claims 122 and 124.

Clark discloses wherein the photoconversion device is a photodiode (col. 2, lines 50-51). However, Clark does not disclose expressly wherein the photoconversion device is a photogate or a photoconductor as claimed in claims 122 and 124, respectively.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to configure the photoconversion device to be a photogate or a photoconductor. Applicant has not disclosed that configuring the photoconversion device to be a photogate or a photoconductor provides an advantage, is used for a particular purpose or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the photodiode taught by Clark or the claimed photogate or photoconductor because both the photogate and photoconductor perform the same function of collecting electric charges based on incident light. Therefore, it would have been obvious to modify Clark to obtain the invention as disclosed in claims 122 and 124.

7. Claims 71-79 and 125-130 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark in view of Mundt as applied to claims 70 and 120 above, and further in view of Burr (US 6,093,951).

Claim 71, Clark in view of Mundt teaches the imager of claim 70, but does not teach wherein said array of pixel sensor cells are formed on a single substrate.

Burr teaches wherein the array of pixel sensor cells and said processor are formed on a single substrate (the above processes are performed at many locations on a single substrate so that multiple MOS devices are formed simultaneously to produce an integrated circuit; col. 16, lines 17-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the single chip of Burr with the imager of Clark as modified by Mundt in order to reduce the conduction path resistance. (See col. 3, lines 40-44 of Burr.)

Claim 72, Burr discloses substantially the claimed invention as set forth in the discussion for claim 72.

Burr does not disclose expressly wherein the CMOS imager is formed on a first substrate, and said processor is formed on a second substrate.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to configure wherein the CMOS imager is formed on a first substrate, and said processor is formed on a second substrate. Applicant has not disclosed that configuring the processor to be formed on a second substrate provides an advantage, is

used for a particular purpose or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the CMOS imager and processor formed on a single substrate taught by Burr or wherein the claimed CMOS imager is formed on a first substrate, and said processor is formed on a second substrate because both designs perform the same function of capturing and processing an image. Therefore, it would have been obvious to modify Burr to obtain the invention as specified in claim 72.

Claim 73, Burr teaches wherein a retrograde well has a dopant concentration within the range of about $1 \times 10^{16}$ to about $2 \times 10^{18}$ atoms per $cm^3$ at the bottom of the retrograde well (col. 8, lines 21-24 of Burr).

Claim 74, Burr teaches wherein a retrograde well has a dopant concentration within the range of about $5 \times 10^{14}$ to about $1 \times 10^{17}$ atoms per $cm^3$ at the top of the retrograde well (col. 8, lines 18-21 of Burr).

Claim 75, Burr teaches wherein a retrograde well has a dopant concentration within the range of about $5 \times 10^{16}$ to about $1 \times 10^{18}$ atoms per $cm^3$ at the bottom of the retrograde well (col. 8, lines 21-24 of Burr).

Claim 76, Burr teaches wherein a retrograde well has a dopant concentration within the range of about 1 x $10^{15}$ to 5 x $10^{16}$ atoms per $cm^3$ at the top of the retrograde well (col. 8, lines 18-21 of Burr).

Claim 77, Burr teaches wherein a retrograde well has a dopant concentration of about 3 x $10^{17}$ atoms per $cm^3$ at the bottom of the retrograde well (col. 8, lines 21-24 of Burr).

Claim 78, Burr teaches wherein a retrograde well has a dopant concentration of about 5 x $10^{15}$ atoms per $cm^3$ at the top of the retrograde well (col. 8, lines 18-21 of Burr).

Claim 79, Burr teaches wherein a retrograde well is a first retrograde well, and said circuit is formed in a second retrograde well (The CMOS retrograde well architecture taught by Burr may be used to construct the circuit disclosed by Clark as modified by Mundt.).

Claim 125, Burr teaches wherein said retrograde well is provided to reflect signal carriers back to the photoconversion device (mobile charge carriers experience less mobility degradation due to impurity scattering; col. 8, lines 26-29 of Burr).

Claim 126, Burr teaches wherein said retrograde well has a vertically graded dopant concentration (col. 8, lines 12-17 of Burr).

Claim 127, Burr teaches wherein said vertically graded dopant concentration of the retrograde well is lowest at a top of the well and highest at a bottom of the well (col. 8, lines 12-17 of Burr).

Claim 128, Burr teaches wherein said vertically graded dopant concentration at the top of the retrograde well is within the range of about $5 \times 10^{14}$ to $1 \times 10^{17}$ atoms per $cm^3$ and the concentration at the bottom of the retrograde well is within the range of about $1 \times 10^{16}$ to $2 \times 10^{18}$ atoms per $cm^3$ (col. 8, lines 18-24 of Burr).

Claim 129, Burr teaches wherein said vertically graded dopant concentration at the top of the retrograde well is within the range of about $1 \times 10^{15}$ to $5 \times 10^{16}$ atoms per $cm^3$ and the concentration at the bottom of the retrograde well is within the range of about $5 \times 10^{16}$ to $1 \times 10^{18}$ atoms per $cm^3$ (col. 8, lines 18-24 of Burr).

Claim 130, Burr teaches wherein said vertically graded dopant concentration at the top of the retrograde well is about $5 \times 10^{15}$ atoms per $cm^3$ and the concentration at the bottom of the retrograde well is about $3 \times 10^{17}$ atoms per $cm^3$ (col. 8, lines 18-24 of Burr).

8. Claim 121 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clark in view of Mundt as applied to claim 120 above, and further in view of Guidash (US 6,657,665).

Claim 121, Clark in view of Mundt teaches the imager of claim 120 but does not teach wherein the photoconversion device further comprises a transfer transistor positioned to gate charges between said photoconversion device to said floating diffusion region.

Guidash teaches, in Figure 4, wherein the photoconversion device further comprises a transfer transistor (transfer gates TG1a) positioned to gate charges between said photoconversion device to said floating diffusion region (col. 4, lines 30-53).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the transfer gates of Guidash with the imager of Clark as modified by Mundt in order to provide an alternate pixel architecture that has a large fill factor, and the capability to perform CDS that also have more linear charge to voltage conversion. (See col. 2, lines 49-53 of Guidash.)

## *Conclusion*

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

### *Inquiries*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHIA-WEI A. CHEN whose telephone number is (571)270-1707. The examiner can normally be reached on Monday - Friday, 7:30 - 17:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chia-Wei A Chen/
Examiner, Art Unit 2622
05/09/2008

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***Supervisory Patent Examiner, Art Unit 2622***